

L Number	Hits	Search Text	DB	Time stamp
-	1	"6576516"	USPAT; US-PGPUB	2003/12/16 14:56
-	1	"6622559"	USPAT; US-PGPUB	2003/12/16 15:01
-	0	10/617269	USPAT; US-PGPUB	2003/12/16 16:38
-	432	(shallow adj trench) with implant\$5	USPAT; US-PGPUB	2003/12/16 16:39
-	278	((shallow adj trench) with implant\$5) and ((shallow adj trench) with oxid\$7)	USPAT; US-PGPUB	2003/12/16 16:41
-	162	((((shallow adj trench) with implant\$5) and ((shallow adj trench) with oxid\$7)) and ((shallow adj trench) with etch\$3)	USPAT; US-PGPUB	2003/12/16 16:54

QRS:  ☒ Plural

Default operator:  ☒ Highlight all hit terms initially

(((shallow adj trench) with implant\$5) and  
 ((shallow adj trench) with oxid\$7)) and ((shallow  
 adj trench) with etch\$3)

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
45	<input type="checkbox"/>	<input type="checkbox"/>	US 6649481 B2	20031118	16	Methods of fabricating a semiconductor device structure for m	438/301	438/201; 438/221;
46	<input type="checkbox"/>	<input type="checkbox"/>	US 6635537 B2	20031021	8	Method of fabricating gate oxide	438/289	257/333; 257/523;
47	<input type="checkbox"/>	<input type="checkbox"/>	US 6624021 B2	20030923	31	Method for forming gate segments for an integrated circuit	438/253	438/254; 438/257
48	<input type="checkbox"/>	<input type="checkbox"/>	US 6624016 B2	20030923	13	Method of fabricating trench isolation structures with extended buffer space	438/221	438/218; 438/294;
49	<input type="checkbox"/>	<input type="checkbox"/>	US 6621119 B1	20030916	19	Isolated stack-gate flash cell structure and its contactless flash memory arra	257/321	257/900
50	<input type="checkbox"/>	<input type="checkbox"/>	US 6621064 B2	20030916	9	CMOS photodiode having reduced dark current and improved light sensit	250/214.1	250/208.1; 257/292;
51	<input type="checkbox"/>	<input type="checkbox"/>	US 6617251 B1	20030909	17	Method of shallow trench isolation formation and planarization	438/691	438/692
52	<input type="checkbox"/>	<input type="checkbox"/>	US 6613626 B1	20030902	10	Method of forming CMOS transistor having a deep sub-micron mid-gap m	438/217	257/369; 257/E21.633;
53	<input type="checkbox"/>	<input type="checkbox"/>	US 6605526 B2	20030813	10	Method of fabricating a semiconductor device	438/257	438/258